5   CLAIMS

1. A decoder (203) comprising a decoding element (208) arranged to operate
   in a first mode for decoding a turbo encoded data stream and in a second
   mode for decoding a viterbi encoded data stream, wherein the decoder

10   (203) is characterised in that the decoding element (208) is responsive to a
       first control signal for switching from the first mode to the second mode
       during decoding of a turbo code block and responsive to a second control
       signal for switching from the second mode to the first mode to allow
       continued decoding of the turbo code block.

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2. A decoder (203) according to claim 1, wherein the decoding element (208)
   is arranged to store data generated during the decoding of the turbo code
   block.

20   3. A decoder (203) according to claim 2, wherein the decoding element (208)
       arranged to retrieve the stored data generated during the decoding of the
       turbo code block to allow continued decoding of the turbo code block.

4. A decoder (203) according to claim 1, wherein the decoding element (208)
25   is arranged to switch from the first mode to the second mode after an
       iteration of the decoding of the turbo code block has been complete.

5. A decoder (203) according to claim 1, wherein the decoding element (208)
   comprises a first logic element that is arranged to calculate forward
30   recursion/backward recursion metrics for a turbo encoded data stream
       when the decoder element is operating in the first mode and to calculate

5   path metrics and survivor path metrics for a viterbi encoded data stream
           when the decoder element is operating in the second mode.

     6. A decoder (203) according to claim 2, wherein the decoding element (208)
         further comprises a second logic unit that is arranged to calculate a
10   posteriori data for a turbo encoded data stream using the forward
         recursion/backward recursion metrics generated by the first logic unit.

     7. A decoder (203) according to claim 2, wherein the decoding element (208)
         further comprises a memory that is arranged to store forward
15   recursion/backward recursion metrics generated by the first logic unit when
         the decoding element (208) is operating in the first mode and to store path
         metrics and survivor path metrics generated by the first logic unit when the
         decoding element (208) is operating in the second mode.